AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method comprising:

disabling selected functions of a computer system in response to an ~~error; and~~ error;

selecting a set of diagnostic instructions based on a history of errors encountered by the computer system;

issuing the set~~a set~~ of diagnostic instructions to a ~~processor~~processor in the computer system; and

incrementally enabling the selected functions until the error is reproduced.

2. (Canceled)

3. (Canceled)

4. (Currently amended) The method of claim 1~~claim 3~~, wherein the selecting further comprises:

selecting the set based on a class of the error.

5. (Original) The method of claim 1, wherein the disabling further comprises:

setting a function disable register that is connected to a plurality of inhibit switches.

6. (Currently amended) An apparatus comprising:

means for disabling selected functions of a computer system in response to an error;

means for selecting a set of diagnostic instructions based on a history of errors encountered by the computer system;

means for issuing the set~~a set~~ of diagnostic instructions to a processor in the computer system; and

means for incrementally enabling the selected functions until the error is reproduced.

7. (Canceled)

8. (Currently amended) The apparatus of claim 6~~claim 7~~, wherein the means for selecting further comprises:

means for selecting the set based on an error class.

9. (Original) The apparatus of claim 6, wherein the means for disabling further comprises:

means for setting a function disable register that is connected to a plurality of inhibit switches.

10. (Currently amended) The apparatus of claim 9, further comprising:

means for saving status of the function disable register and the error in a ~~history~~history table after the error is reproduced.

11. (Currently amended) A storage~~signal bearing~~ medium encoded with instructions, wherein the instructions when executed comprise:

detecting an error;

disabling selected functions of a computer system in response to the error;

selecting a set of diagnostic instructions based on a history of errors encountered by the computer system;

issuing the set~~a set~~ of diagnostic instructions to a processor; and

incrementally enabling the selected functions until the error is reproduced.

12. (Canceled)

13. (Currently amended) The storage~~signal-bearing~~ medium of claim 11~~claim 12~~, wherein the selecting further comprises:

selecting the set based on an error class.

14. (Currently amended) The storage~~signal-bearing~~ medium of claim 11, wherein the disabling further comprises:

setting a function disable register that is connected to a plurality of inhibit switches.

15. (Currently amended) The storage~~signal-bearing~~ medium of claim 14, further comprising:

saving status of the function disable register and the error in a ~~history~~history table after the error is reproduced.

16. (Currently amended) A computer system comprising:

a processor;

a sequence pad control register to introduce delay into selected operations of the computer system;

a plurality of inhibit switches to selectively enable and disable a corresponding plurality of functions of the processor;

a function disable register to control the plurality of inhibit switches; and

a shift unit to incrementally change the contents of the function disable register.

17. (Canceled)

18. (Currently amended) The computer system of claim 16~~claim 17~~, further comprising:

a diagnostic history entry comprising contents of a failing instruction address register, contents of the function disable register, and contents of the sequence pad register.

19. (Original) The computer system of claim 16, further comprising:

a memory connected to the processor; and

an additional inhibit switch to selectively enable and disable a function of the memory, wherein the function disable register is to control the additional inhibit switch.

20. (Original) The computer system of claim 16, further comprising:

a bus connected to the processor; and

an additional inhibit switch to selectively enable and disable a function of the bus, wherein the function disable register is to control the additional inhibit switch.